

AT32F4xx Timer Parallel Synchronization Mode

Introduction

This sample code demonstrates how to configure parallel synchronization among three timers.

Applicable products:

Product series	AT32Fxx series
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List of major peripherals used:

Peripherals	TIMER
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1 Quick start

1.1 Hardware resources

AT-START-F403A V1.0 evaluation board

1.2 Software resources

1. This Demo is based on AT32F403A, and AT32F403A_407_Firmware_Library_V2.x.x (BSP version)
2. TMR2 is used as a master timer, and an overflow event acts as a TRGOUT source to trigger two slave timers.

TMR3 and TMR4 are slave timers. They are used to synchronize with the master time in Suspend mode.

Enable the compare output feature of TMR2_CH1, TMR3_CH1 and TMR4_CH1 to generate PWM. TMR2_CH1 output frequency is 750 KHz, 20% duty cycle; TMR3_CH1 output frequency is 75 KHz, 30% duty cycle; TMR4_CH1 output frequency is 150 KHz, 60% duty cycle.

1.3 Example case

- 1) Use oscilloscope to TMR2_CH1 (PA0), TMR3_CH1 (PA6) and TMR4_CH1 (PB6)

Table 1. Document revision history

Date	Revision	Changes
2021.12.03	2.0.0	Initial release

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